Code No: R201216 **R20** SET - 1

I B. Tech II Semester Regular Examinations, September- 2021

COMPUTER ORGANIZATION

(Com. To CSE, IT)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1. a) Explain how Hamming Code is used for Error Correction. (7M)
   b) Compare r's complement and (r-1)'s complement by taking two examples. (7M)

Or

2. a) Discuss the significance of ASCII code with few examples. (7M)
   b) What is fixed point Representation? Explain with examples. (7M)

UNIT-II

3. a) Explain how a half-adder can be realized by using one X-OR gate and one AND gate. (7M)
   b) Explain the combinatorial circuit design with an example. (7M)

Or

4. a) Explain the disadvantage of constructing a full adder with two half adders. (7M)
   b) Discuss the features of the Ring counter with an example. (7M)

UNIT-III

5. a) Explain the hardware implementation of the Binary multiplier. (7M)
   b) What are the features of the decimal athemetic unit? Explain the same with an example. (7M)

Or

6. a) Construct the flow chart and explain the division algorithm with an example. (7M)
   b) What are the various floating-point arithmetic operations available? Explain the same with an example. (7M)

UNIT-IV

7. a) State the purpose of the micro program with an example. (7M)
   b) Explain the implementation of do-while, repeat-until with an example. (7M)

Or

8. a) What are the steps involved in the design of the control unit? Explain. (7M)
   b) Explain how string operations can be performed in 8086. Discuss the importance of far and near procedures with suitable examples. (7M)

UNIT-V

9. a) Explain the various elements of cache design in detail. (7M)
   b) A two-way set associate cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte-addressable. Show the format of primary memory addresses. (7M)

Or

10 a) A set-associative cache consists of 64 lines or slots, divided into four-line sets. Main memory consists of 4K blocks of 128 words each. Show the format of main memory addresses. (7M)
   b) Explain the process of asynchronous data transfer with an example. (7M)
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